APPLICATION

OF

Nathan R. Carter

**FOR**

UNITED STATES LETTERS PATENT

**ON**

A COMMON MODE LINEARIZED INPUT STAGE AND
AMPLIFIER TOPOLOGY

Docket No. A8SJ2357US

**Assigned to:**

ANALOG DEVICES, INC.

# A COMMON MODE LINEARIZED INPUT STAGE AND
# AMPLIFIER TOPOLOGY

<u>BACKGROUND OF THE INVENTION</u>
<u>Field of the Invention</u>

This invention relates to the field of operational amplifiers (op amps) input stages, and particularly to
5   common mode linearized input stages.

<u>Description of the Related Art</u>

The open loop gain of an op amp decreases with increasing input signal frequency. This requires that a
10  larger error signal appear across the amplifier's input for signals of a given amplitude and increasing frequency. This, in turn, requires the op amp to have a large linear input range; if the input range is insufficient, distortion will result.

15  A bipolar differential transistor pair has a highly nonlinear input range. One way to extend the linear portion of a bipolar pair's input range is with the use of degeneration resistors. However, the use of degeneration resistors can result in noise degradation, as well as loss
20  of headroom.

Another approach to extending linear input range requires the use of class AB-type input stages. Unfortunately, such stages are also known to increase noise and lower precision.

25  Yet another approach to extending linear input range is to use a series-connected doublet configuration which employs the "multi-tanh principle", as described, for example, in *Gilbert*, IEEE Journal of Solid-State Circuits, Volume 33, Issue 1, Jan. 1998, pp. 2-17. Here, individual
30  nonlinear (hyperbolic tangent, or tanh) transconductance

functions can be separated along the input-voltage axis to achieve a much more linear overall function. A typical implementation is shown in FIG. 1. However, though this arrangement extends the linear input range, it requires

5 dividing resistors $R_a$ and $R_b$ between its inputs.

An op amp's linear input range can also be affected by manipulating its tail currents. One tail-current modulating approach is described in U.S. Patent No. 5,214,329 to Furino, Jr. Here, the amplifier's bias currents are

10 modulated as a function of the differential input voltage. However, Furino modulates bias currents through a direct measurement of differential input voltage, which can add current noise and offset current to the differential inputs.

15

SUMMARY OF THE INVENTION

A common mode linearized input stage and an amplifier topology are presented which overcome the problems noted above, providing a large linear input range, fast slew

20 rate, and low noise.

The present input stage comprises an NPN differential transistor pair having its emitters connected together at a first common node, and its bases connected to receive a differential input signal. Similarly, a PNP differential

25 transistor pair has its emitters connected together at a second common node, and its bases connected to the differential input signal. The NPN and PNP differential pairs are biased with respective tail currents provided to the first and second common nodes by first and second tail

30 current sources, respectively.

The input stage includes a tail current modulation circuit which generates complementary output currents as a function of the voltage difference between the first and second common nodes. The first and second tail current

35 sources are connected to receive respective complementary

output currents, and are arranged to generate their respective tail currents as a function of their complementary output currents.

The tail current modulation circuit is arranged to
5 reduce the magnitude of the tail currents provided to the differential transistor pairs when the differential input signal is zero, and to allow the tail currents to increase with an increasing differential input signal. When properly arranged, this technique serves to extend the input pairs'
10 linear input range.

The tail current modulation circuit preferably comprises a PNP diversion transistor having its base connected to the first common node, its collector coupled to the first tail current source, and its emitter connected
15 to a third common node, and a NPN diversion transistor having its base connected to the second common node, its collector coupled to the second tail current source, and its emitter connected to the third node. The PNP and NPN diversion transistors conduct and thereby divert the first
20 and second tail currents from the NPN and PNP differential transistor pairs, respectively, when the differential input signal is zero - with the tail currents being reduced by a scaling factor set by the ratio of the diversion transistors' emitter size to the input pairs' emitter size.
25 However, in the presence of a non-zero differential input signal, the NPN and PNP differential pairs pull the voltages at the first and second common nodes closer together, which eventually turns off the diversion transistors and allows the full tail currents to flow
30 through the input pairs. In addition to linearizing the input stage, this arrangement provides a substantial increase in slew rate over a simple differential pair having a comparable transconductance. In addition, all current noise from the diversion transistors is common
35 mode, as is noise generated by the tail current sources

that drive the input devices. In addition, the early voltage of the diversion transistors track with the differential input pairs, resulting in increased power supply rejection ratio (PSRR) and common mode rejection
5   ratio (CMRR). The scaling factor can also be selected such that the input stage decompresses the differential input signal, to compensate for possible compression caused by later stages within the amplifier.

The present input stage produces differential output
10  currents, which are preferably coupled to an input stage mirroring structure. The differential output currents are provided to complementary mirrors that are fed by a single floating current source and produce a single-ended output current. Noise due to the current source is correlated for
15  the two mirrors, such that its noise sums to zero at the output. The present input stage is connected to the mirroring structure in a balanced fashion, so that an equal current on both sides of the mirror causes the mirrors to shift up and down without changing the output current -
20  thereby rejecting common mode noise.

Further features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings.
25

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a prior art series-connected doublet.

FIG. 2 is a schematic/block diagram of a common mode
30  linearized input stage per the present invention.

FIG. 3 is a schematic diagram of a preferred embodiment of the present common mode linearized input stage.

FIG. 4 is a graph of input stage transconductance vs.
35  differential input voltage for a common mode linearized

input stage per the present invention.

FIG. 5 is a schematic diagram of an alternative embodiment of a common mode linearized input stage per the present invention.

5      FIG. 6 is a schematic diagram of an embodiment of a single-ended version of a common mode linearized input stage per the present invention.

FIG. 7 is a block diagram of an amplifier topology which includes the present input stage coupled to an input

10     stage mirroring structure.

FIG. 8 is a schematic diagram of a preferred embodiment of a common mode linearized input stage and input stage mirroring structure per the present invention.

FIG. 9 is a schematic diagram of a alternative

15     embodiment for an input stage mirroring structure per the present invention.

FIG. 10 is a schematic diagram of a preferred embodiment of a bias current source per the present invention.

20

DETAILED DESCRIPTION OF THE INVENTION

The basic principles of a common mode linearized input stage per the present invention are shown in FIG. 2. A NPN differential transistor pair Q1/Q2 have their emitters

25     connected together at a common node 10 and their bases connected to respective input terminals $V_{in+}$ and $V_{in-}$, which receive a differential input signal having a differential voltage $V_d$. A tail current source 12 provides a tail current $I_{tail1}$ to common node 10, and Q1 and Q2 conduct respective

30     output currents $I_{D1+}$ and $I_{D1-}$ in response to an applied differential input signal.

Similarly, a PNP differential transistor pair Q3/Q4 have their emitters connected together at a common node 14 and their bases connected to input terminals $V_{in-}$ and $V_{in+}$,

35     respectively. A tail current source 16 provides a tail

current $I_{tail2}$ to common node 14, and Q3 and Q4 conduct respective output currents $I_{D2+}$ and $I_{D2-}$ in response to an applied differential input signal.

The input stage also includes a tail current modulation circuit 17 which generates complementary output currents $I_{in1}$, $I_{in2}$ as a function of the difference between the voltage at common node 14 ($V_{14}$) and the voltage at common node 10 ($V_{10}$). Tail current sources 12 and 16 are connected to receive complementary output currents $I_{in1}$ and $I_{in2}$, respectively, and are arranged to generate their respective tail currents $I_{tail1}$ and $I_{tail2}$ as a function of their complementary output currents; i.e., $I_{tail1}$ is a function of $I_{in1}$, and $I_{tail2}$ is a function of $I_{in2}$.

Tail current modulation circuit 17 is arranged to reduce the magnitudes of tail currents $I_{tail1}$ and $I_{tail2}$ when the differential input voltage $V_d$ is zero (i.e., when $|V_{14}-V_{10}|$ is at its maximum value), and to allow the tail currents to increase up to their maximum available values for an increasing differential input signal (as the magnitude of $|V_{14} - V_{10}|$ falls). When tail current modulation circuit 17 and tail current sources 12 and 16 are properly arranged, the input pairs' linear input range may be extended.

A preferred embodiment of a common mode linearized input stage is shown in FIG. 3. As in FIG. 2, NPN differential pair Q1/Q2 have their emitters connected together at common node 10, and PNP differential pair Q3/Q4 have their emitters connected together at common node 14, with the bases of both pairs connected to input terminals $V_{in-}$ and $V_{in+}$. Tail current sources 12 and 16 provides respective tail currents (identified here as simply "$I_{tail1}$" and "$I_{tail2}$") to common nodes 10 and 14, respectively. In response to an applied differential input signal, Q1 and Q2 conduct respective output currents $I_{D1+}$ and $I_{D1-}$, and Q3 and Q4 conduct respective output currents $I_{D2+}$ and $I_{D2-}$.

Tail current modulation circuit 17 is preferably implemented with a pair of "diversion" transistors Q5 and Q6. Q5 is an NPN transistor having its base connected to node 14, its collector connected to tail current source 16,

5    and its emitter connected to a node 18. Q6 is a PNP transistor having its base connected to node 10, its collector connected to tail current source 12, and its emitter connected to node 18.

This configuration results in Q6 and Q5 conducting

10   currents $I_{in1}$ and $I_{in2}$ such that they vary as a function of the difference between the voltages at node 14 and node 10 ($V_{14}$ - $V_{10}$). When the input stage is in a balanced state - i.e., with a differential input voltage $V_d$ of zero - node 18 is at the differential input signal's common mode voltage

15   $V_{cm}$, the voltage at common node 14 is one base-emitter voltage above $V_{cm}$, and the voltage at common node 10 is one base-emitter voltage below $V_{cm}$. As such, diversion transistors Q6 and Q5 both conduct and thereby divert tail currents $I_{tail1}$ and $I_{tail2}$ from the NPN and PNP differential

20   input pairs. However, when a non-zero $V_d$ is applied to $V_{in+}$ and $V_{in}$, NPN input pair Q1/Q2 pull up the voltage at node 10, and PNP input pair Q3/Q4 pull down the voltage at node 14, thereby reducing the base-emitter voltages of Q5 and Q6 and, if $V_d$ is large enough, causing them to turn off. This

25   allows the tail currents $I_{tail1}$ and $I_{tail2}$ flowing through the input pairs to be as large as possible. In a large signal sense, this will result in a substantial increase in slew rate when compared with a simple differential pair having an equivalent input transconductance.

30   The diversion transistors are preferably differently-sized than the input pair transistors. Assume that Q1-Q4 have an emitter size of 1, Q5 and Q6 have an emitter size of A, and the maximum possible values for $I_{tail1}$ and $I_{tail2}$ (i.e., with Q5 and Q6 off) are equal to "$I_{1(max)}$" and

35   "$I_{2(max)}$", respectively. Then, when Q5 and Q6 are on, they

remove tail current from Q1-Q4 by a ratio proportional to
A. When so arranged, the current $I_{D1+}$ conducted by NPN
transistor Q1 is given by:

$$I_{D1+} = \frac{e^{\alpha}}{e^{\alpha} + A + e^{-\alpha}} * I_{1(max)},$$

5    the current conducted by NPN transistor Q2 is given by:

$$I_{D1-} = \frac{e^{-\alpha}}{e^{\alpha} + A + e^{-\alpha}} * I_{1(max)},$$

and the current $I_{div}$ conducted by diversion transistors Q5
and Q6 is given by:

$$I_{div} = \frac{A}{e^{\alpha} + A + e^{-\alpha}},$$

10   where $\alpha$ is given by:

$$\alpha = \frac{V_{in+} - V_{in-}}{2 * V_t},$$ where $V_t$ is the thermal voltage $kT/q$.

Similarly, the current $I_{D2+}$ conducted by PNP transistor Q3
is given by:

$$I_{D2+} = \frac{e^{\alpha}}{e^{\alpha} + A + e^{-\alpha}} * I_{2(max)},$$

15   and the current conducted by PNP transistor Q4 is given by:

$$I_{D2-} = \frac{e^{-\alpha}}{e^{\alpha} + A + e^{-\alpha}} * I_{2(max)}.$$

Taking the different between the two output currents,
and then the derivative of the result, results in an
expression for input stage transconductance $G_m$ as follows:

20   $$G_m = \frac{2A * \cosh\alpha + 4}{(2 * \cosh\alpha + A)^2} \bullet \frac{d\alpha}{d(V_{in+} - V_{in-})} \bullet I_{(max)}$$

(assuming $I_{1(max)} = I_{2(max)} = I_{(max)}$).
A graph of transconductance versus differential input
voltage $V_d$ for various values of A is shown in FIG. 4. This
graph demonstrates the present invention's ability to, by
25   properly selecting a value for A, create not only a flat
input transconductance and thereby linearize the input
pairs, but also to create a transconductance that

"decompresses" the input signal - i.e., gives the input stage an input gain that increases with $V_d$ - to compensate for possible compression caused by later stages within the amplifier. As seen in FIG. 4, values for A of 4 or greater are preferred, as these values provide either a flat response or a response which decompresses the input signal.

Another benefit of using the present structure is that all current noise from diversion transistors Q5 and Q6 is common mode, as is noise from the tail current sources 12 and 16, just as in a single differential input pair. The remaining noise sources are those inherent in devices Q1/Q2 and Q3/Q4, such as base resistance and shot noise. In addition, the early voltage of devices Q5 and Q6 tracks with the differential input devices Q3/Q4 and Q1/Q2. Due to this tracking, there is in no common mode modulation of tail current based on early voltage effects of the diversion transistors. This results in increased PSRR and CMRR.

Note that the linear input range of the input stage shown in FIG. 3 could be extended even further with the use of degeneration resistors, respective ones of which would be connected in series with the emitters of Q1-Q6.

Tail current sources 12 and 16 can be implemented in a number of different ways. In FIG. 3, tail current source 12 comprises a fixed current source 20 which generates an output current $I_{1(max)}$, and a bias transistor Q7 which is biased with a voltage $V_{bias1}$. Q7's emitter is connected to fixed current source 20 at a node 22, and its collector is connected to node 10 such that Q7 conducts $I_{tail1}$. The collector of diversion transistor Q6 is connected to node 22 such that, when Q6 is off, $I_{tail1}$ is equal to $I_{1(max)}$. However, when Q6 is on, some of $I_{1(max)}$ is diverted by Q6, thereby reducing $I_{tail1}$ such that $I_{tail1} = I_{1(max)} - I_{in1}$.

Similarly, tail current source 16 comprises a fixed current source 24 which generates an output current $I_{2(max)}$,

and a bias transistor Q8 which is biased with a voltage $V_{bias2}$. Q8's emitter is connected to fixed current source 24 at a node 26, and its collector is connected to node 14 such that Q8 conducts $I_{tail2}$. The collector of diversion transistor Q5 is connected to node 26 such that, when Q5 is off, $I_{tail2}$ is equal to $I_{2(max)}$. However, when Q5 is on, some of $I_{2(max)}$ is diverted by Q5, thereby reducing $I_{tail2}$ such that $I_{tail2} = I_{2(max)} - I_{in2}$. Bias voltages $V_{bias1}$ and $V_{bias2}$ are typically set no more that a few base-emitter voltages above the most negative rail (VEE) and a few base-emitter voltages below the most positive rail (VCC), respectively.

Note that the simplest implementation of current sources $I_{2(max)}$ and $I_{1(max)}$ uses a single resistor for each and the appropriate selection of $V_{bias2}$ and $V_{bias1}$.

An alternative implementation for tail current sources 12 and 16 is shown in FIG. 5. For tail current source 12, a fixed current source 30 provides an output current $I_{max}$ to a first current mirror comprising a diode-connected input transistor Q9 and an output transistor Q10; the bases of Q9 and Q10 are connected together at a node 32. Transistors Q9 and Q10 are connected to mirror $I_{max}$ to node 10, such that Q10 conducts $I_{tail1}$. A second current mirror comprises a diode-connected input transistor Q11 and an output transistor Q12. Transistor Q11 is connected to mirror the current conducted by diversion transistor Q6 (i.e., $I_{in1}$) to Q12, which is connected to node 32. When so arranged, when Q6 is off, $I_{tail1}$ is equal to $I_{max}$ (assuming Q9:Q10=1:1). However, when Q6 is on, some of $I_{max}$ is diverted from mirror transistor Q9, thereby reducing the $I_{max}$ current mirrored to node 10 - and thus reducing $I_{tail1}$.

Similarly, for tail current source 16, output current $I_{max}$ is provided to a third current mirror comprising a diode-connected input transistor Q13 and an output transistor Q14; the bases of Q13 and Q14 are connected together at a node 34. Transistors Q13 and Q14 are

connected to mirror $I_{max}$ to node 14, such that Q14 conducts
$I_{tail2}$. A fourth current mirror comprises a diode-connected
input transistor Q15 and an output transistor Q16.
Transistor Q15 is connected to mirror the current conducted
5  by diversion transistor Q5 (i.e., $I_{in2}$) to Q16, which is
connected to node 34. When so arranged, when Q5 is off,
$I_{tail2}$ is equal to $I_{max}$ (assuming Q13:Q14=1:1). However, when
Q5 is on, some of $I_{max}$ is diverted from mirror transistor
Q13, thereby reducing the $I_{max}$ current that is mirrored to
10  node 14 - and thus reducing $I_{tail2}$.

The tail current sources shown in FIG. 5 might be
preferred in that they provide more flexibility than those
shown in FIG. 3. Here, the Q11/Q12 and Q15/Q16 current
mirrors can be sized as needed (size "B"), and the Q9/Q10
15  and Q13/Q14 current mirrors can be sized as needed (size
"C"), to provide desired slew rate, current consumption,
and/or common mode noise characteristics. Making the
product of A, B and C = 4 provides the flattest response.
In addition, this arrangement enables Q5 and Q6 to be
20  scaled down and $I_{max}$ to be made dynamic so that it need
only be large when a large differential input voltage is
applied to $V_{in+}$ and $V_{in-}$. This type of input stage should be
limited to use in low noise applications. In low noise
applications, the input devices are typically large; this
25  would result in Q5 and Q6 being very large (A times larger)
using the FIG. 3 implementation; such a configuration
typically has a correspondingly large current
consumption. Here, Q5 and Q6 need only be A/B*C the size of
the input devices, saving both area and current.

30  A single-ended version of the present invention is
shown in FIG. 6. As before, the NPN and PNP differential
transistor pairs Q1/Q2 and Q3/Q4 are connected to input
terminals $V_{in+}$ and $V_{in-}$. The emitters of Q1/Q2 are connected
to common node 10, and the emitters of Q3/Q4 are connected
35  to common node 14. Here, however, the collectors of Q3/Q4

do not provide a differential output current, but are instead connected to supply voltage VEE. The connections of diversion transistors Q5 and Q6 are largely the same, with the bases of Q6 and Q5 connected to nodes 10 and 14, respectively, and their emitters connected together at a common node 40.

A tail current source 42 providing an output current I1 is connected to node 10, and a current source 44 providing an output current I2 is connected to node 14. The collector of diversion transistor Q6 is connected to current source 42. Here, however, the collector of diversion transistor Q5 is connected to supply voltage VCC.

In operation, output current I2 in combination with the common mode voltage $V_{cm}$ establishes a voltage at node 14. The resulting current in Q5 and Q6 subtracts tail current from input pair Q1/Q2. It should be noted that, when the FIG. 6 circuit is arranged for a response with maximal flatness, the stage's linear input range is half that of the fully complementary embodiment shown in FIG. 2 - unless a proportional current (not shown) is subtracted from I2.

The present common mode linearized input stage is preferably coupled to an input stage mirroring structure as shown in FIG. 7. NPN input pair Q1/Q2 produces differential output currents $I_{D1+}/I_{D1-}$, which are coupled to balanced nodes on each side of a current mirror circuit 45. The PNP input pair produces differential output currents $I_{D2+}/I_{D2-}$, which are coupled to balanced nodes on each side of a current mirror circuit 46 which is complementary to current mirror circuit 45. The complementary current mirror circuits are fed by a single floating current source 47 and produce a single-ended output current $I_{out}$ at an output node 48. A compensation capacitor $C_{comp}$ is preferably connected between output node 48 and ground. Noise due to current source 47 is correlated for the two mirror

circuits, such that its noise sums to zero at the output.

The present input stage is connected to the mirroring structure in a balanced fashion: i.e., with $I_{D1+}$ and $I_{D1-}$ connected across current mirror circuit 45, and $I_{D2+}$ and $I_{D2-}$

5    connected across current mirror circuit 46. If there is a variation in $I_{tail1}$, $I_{D1+}$ and $I_{D1-}$ are affected equally such that the balanced nodes on each side of mirror circuit 45 go up or down by equal amounts, with no resulting change in output current $I_{out}$. Similarly, if $I_{tail2}$ varies, $I_{D2+}$ and $I_{D2-}$

10    are affected equally such that the balanced nodes on each side of mirror circuit 46 go up or down by equal amounts, without affecting output current $I_{out}$. In this way, common mode noise is rejected. Since differential output currents $I_{D1+}/I_{D1-}$ and $I_{D2+}/I_{D2-}$ inject offset currents into mirror

15    circuits 45 and 46, respectively, which are otherwise balanced, output current $I_{out}$ only varies when $I_{D1+}$ and $I_{D1-}$, or $I_{D2+}$ and $I_{D2-}$, are unequal.

A preferred embodiment of an input stage mirroring structure is shown in FIG. 8. Differential currents $I_{D1+}$ and

20    $I_{D1-}$ are connected to current mirror circuit 45 at nodes 50 and 52, respectively, which are also connected to supply voltage VCC via a pair of degeneration resistors; mirror circuit 45 also includes a current mirror made from PNP input and output transistors Q17 and Q18, respectively,

25    connected between nodes 50 and 52. Similarly, differential currents $I_{D2+}$ and $I_{D2-}$ are connected to current mirror circuit 46 at nodes 54 and 56, respectively, which are also connected to supply voltage VEE via a pair of degeneration resistors; mirror circuit 45 also includes a current mirror

30    made from NPN input and output transistors Q19 and Q20, respectively, connected between nodes 54 and 56. Floating current source 47 produces a bias current $I_{bias}$, which is connected to mirror output transistor Q18 at a node 59, and to mirror output transistor Q20 at a node 60. Current

35    mirror circuit 45 also includes a PNP output transistor

Q21, which has its base connected to node 59, its emitter connected to Q17 and its collector connected to output node 48. Current mirror circuit 46 also includes a NPN output transistor Q22, which has its base connected to node 60,

5    its emitter connected to Q19 and its collector connected to output node 48. A compensation capacitor $C_{comp}$ is preferably connected between output node 48 and ground. A buffer or output stage 64 may be connected to output node 48 to produce an overall output voltage $V_{OUT}$.

10      In operation, the mirroring structure provides an output voltage $V_{out}$ and an output current $I_{out}$ at node 48, both of which vary with $I_{D1+}$, $I_{D1-}$, $I_{D2+}$ and $I_{D2-}$. An increase in $I_{D2-}$ (for example) causes the voltage at node 56 to increase. Neglecting all base currents, mirror output

15    transistor Q22 forms a loop with input transistor Q19 and output transistor Q20, forcing Q20's output current to equal $I_{bias}$ for all differential input values of $I_{D2+}$-$I_{D2-}$. This causes the $V_{be}$ of Q20 to be constant, and the voltage at the base/collector of Q19 to track with the increasing

20    voltage at node 56. As the base/collector of Q19 increases, the emitter of Q19 must also increase, causing more current to flow in Q19 and Q22. This current flow is aided by the corresponding drop of $I_{D2+}$, which decreases with increasing $I_{D2-}$. Similarly, the voltage at node 56 decreases with

25    decreasing $I_{D2-}$, causing the base/collector of Q19 to decrease. Q20's $V_{be}$ is constant, so the emitter of Q19 decreases, along with the current flowing through Q19 and Q22. $I_{D2+}$ increases with decreasing $I_{D2-}$, causing the current in Q19 and Q22 to decrease further. Mirror circuit 45

30    operates in a complementary fashion to mirror 46.

     The structure shown provides a high gain-producing output impedance, good input stage headroom, good recovery after slew, and low inherent noise. Due to the balanced connection of the input stage into the Q17/Q18 and Q19/Q20

35    mirrors, the integrity of the differential input path is

maintained, which enables the common mode noise of the input stage to be rejected. The peak output current for slewing is not limited by the size of $I_{bias}$, which permits a fairly low $I_{bias}$ current to produce high output slew

5  currents. Here, the peak output current is only limited by the peak value of the tail currents $I_{tail1}$ and $I_{tail2}$.

Several factors should be considered when selecting the value of $I_{bias}$. If $I_{bias}$ is too low, the input signal would be extremely compressed by the mirroring structure,

10  and the structure's transistors would operate at less than their peak speed. But if $I_{bias}$ is too high, current consumption may be unacceptably high.

One drawback to the mirroring structure shown in FIG. 8 is that it tends to compress a linear input current. When

15  the input stage is balanced ($I_{D1+} = I_{D1-}$, $I_{D2+} = I_{D2-}$), the current densities in the current mirror transistors Q17/Q18 and Q19/Q20 are equal, the current out of each complementary mirror is equal to $I_{bias}$, and $I_{out} = 0$. However, when non-zero differential currents are applied to the

20  mirroring structure, the current densities in the mirror transistors become unequal, which causes the differential input current to be compressed; i.e., $I_{out}$ changes less and less for an increasing differential input current.

One method to limit the compression would be to

25  increase $I_{bias}$ until the desired level of linearity is reached. This has the drawback of using substantially more current than actually necessary, and possibly increasing the voltage drop across the degeneration resistors to an unacceptable level. Alternatively, $I_{bias}$ could be increased

30  dynamically based on the size of the differential input voltage, but this has the negative effect of creating a slope to the linear region of the input transconductance in the presence of reasonable device mismatch, which would appear as second harmonic distortion on the output since

35  the transconductance is not balanced on both sides of zero.

Thus, the preferred method of compensating for the mirroring structure's compression is to select a value for the input stage's scaling ratio A that causes the input stage to decompress the differential currents a corresponding amount, thereby producing a linear output current at the output node 48 of the amplifier.

One possible alternative implementation for the input stage mirroring structure is shown in FIG. 9. Here, the differential currents $I_{D1+}/I_{D1-}$, $I_{D2+}/I_{D2-}$ are connected on the opposite sides of the Q17/Q18 and Q19/Q20 current mirrors: $I_{D1+}$ is connected to the collector of Q18 and $I_{D1-}$ is connected to a node 70 at the junction of Q17 and Q21, while $I_{D2+}$ is connected to a node 72 at the junction of Q19 and Q22 and $I_{D2-}$ is connected to the collector of Q20. Two additional transistors Q23 and Q24 are preferably paired with Q21 and Q22, respectively, to balance the voltages in mirror circuits 45 and 46. When so arranged, the current in output transistor Q22 is given by:

$I_{Q22} = I_{bias} - (I_{D2+} - I_{D2-})$,

the current in output transistor Q21 is given by:

$I_{Q21} = I_{bias} - (I_{D1-} - I_{D1+})$,

and the output current is given by:

$I_{out} = I_{Q21} - I_{Q22} = I_{D2+} + I_{D1+} - I_{D2-} - I_{D1-})$

Here, the mirror transistor currents are equal (i.e., $I_{Q19}=I_{Q20}$, $I_{Q17}=I_{Q18}$) as long as the applied differential currents (i.e., $I_{D1+}-I_{D1-}$, $I_{D2+}-I_{D2-}$) are less than $I_{bias}$. With equal currents in the mirror devices, there is no compression of the differential input currents. However, this arrangement may suffer from overload problems when the amplifier is slewing.

Note that the input stage mirroring structures shown in FIGs. 8 and 9 are merely exemplary. A mirroring structure as shown in FIG. 7, having complementary mirrors fed by a single floating current source, could be implemented in a number of different ways - many of which

would be suitable for use with the present input stage.

Note also that the present common mode linearized input stage is not limited to use with the mirroring structures depicted. Though the mirroring structures shown
5   work well with the present input stage, advantages are provided by the common mode linearized input stage regardless of the nature of the following stage.

A preferred implementation of current source 47 is shown in FIG. 10. A PNP transistor Q23 and an NPN
10  transistor Q24 are connected in series via a resistor R1. A reference voltage $V_{ref1}$ is connected between the bases of Q23 and Q24, and a reference voltage $V_{ref2}$ is connected between ground and the base of Q23, such that Q23 and Q24 conduct bias current $I_{bias}$. When arranged as shown, the current noise
15  that comes out of both ends of the structure is correlated, so that the noise on the output sides of the Q17/Q18 and Q19/Q20 current mirrors sums to zero.

While particular embodiments of the invention have been shown and described, numerous variations and alternate
20  embodiments will occur to those skilled in the art. Accordingly, it is intended that the invention be limited only in terms of the appended claims.